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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,594	10/23/2003	Benoit Nadeau-Dostie	LVPAT066US	6739

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,594	NADEAU-DOSTIE ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-40 and 56* is/are allowed.

6)☒ Claim(s) *1-31 and 41-54* is/are rejected.

7)☒ Claim(s) *55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application filed 10/23/2003. Claims 1-56 are presently under examination and still pending in the Application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) to CANADA 2,414,632, filed 12/18/2002. The certified copy has been filed in parent Application No. 10/690,594, filed on 10/23/2003.

Drawings

The drawings received on March 5, 2004, for Replacement Sheets 4-6, are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-31, 41-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Heaslip et al. (US-Patent 6,643,807) issued: November 4, 2003; filed: August 1, 2000.

Regarding independent Claims 1-31, 41-54, Heaslip discloses a method and apparatus including an array-built-in-self-test (ABIST) for efficient, fast, bitmapping of large embedded arrays in manufacturing test, which allows for bitmapping at speed, such as in real time, with the use of on chip clock generation (OPCG) with a phase lock loop (PLL) to clock the array BIST at high speeds. To map the failing array's with AC faults, Heaslip uses on chip BIST clock gating that immediately disables the clocks when the BIST compare circuitry detects a fail, which is then detected at the external tester pin a few cycles after it occurred. This allows the tester to run and detect fails at its slower speeds. The tester detects the fails and scans the diagnostic register for the failing address and data information, (see, Fig. 1 and Col. 2, lines 40-64). The method and apparatus comprising:

An embedded DRAM or SRAM under test for testing each memory cell of a row or column according to a memory test algorithm (from address and data generator 210 and 220, respectively) under the control of a first clock (BIST clock 241) generated by the on chip clock generation (OPCG) clock generator 240, which clocks the array BIST at high speeds.

Generating a failure summary (bitmapping at speed) using a read compare register 255 to compare the data read back from the arrays to the data written and a diagnostic register 251 to capture the compare output and failing address. The comparator identifies failed cycles where the retrieved data does not correspond

correctly to the test data, and the diagnostic unit stores the failed cycles and being responsive to the controller regenerating and re-storing the test data in the read/write memory and stores the failed data and failing addresses.

Transferring the failure summary from the circuit under control of a second clock (tester external clock). The fail is detected at the external tester pin a few cycles after it occurred. This allows the tester to run and detect fails at its slower speeds. The tester detects the fails and scans the diagnostic register for the failing address and data information. Upon a completion of the fail data collection, the tester asserts the internal BIST clock back on and continues to the next failing address.

Allowable Subject Matter

Claims 32-40, 56 are allowed.

Claim 55 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious a method, as recited in the independent claim 32, including among other limitations, "classifying the detected failure according to predetermined failure types, and updating a failure mask register with results of comparisons of memory outputs and expected memory outputs".

Independent claim 56 recites, a memory test controller, including among other limitations, "failure type identification means responsive to a failure mask for classifying detected failures according to predetermined failure types, and counter means responsive to outputs of said failure type identification means for counting failures of each the predetermined types".

Also, claim 55 recites among other limitations, "a failure type identification circuit for determining a failure type of each detected failure, a failure type counter for each of said predetermined failure type, and a failure mask register for storing results of comparisons between each memory output and corresponding expected memory outputs".

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schwarz (US 6,496,947), Built-in-self-repair circuit with pause for data retention coverage.

Stubbs (US 6,286,115), On-chip testing circuit and method for integrated circuits.

Adams et al. (US 5,912,901), Method and built-in self-test apparatus for testing an integrated circuit which capture failure information for a selected failure.

Chen et al. (US 6,421,794), Method and apparatus for diagnosing memory using self-testing circuits.

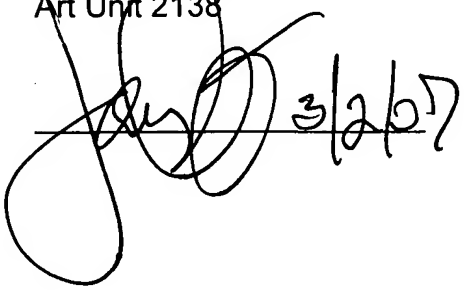
Kalter et al. (US 5,961,653), Processor based BIST for an embedded memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



Date: 2 March 2007
Office Action: Non-Final Rejection

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